Amendments to the Specification:

Please replace the title with the following new title:

~~METHOD OF MANUFACTURING~~ SEMICONDUCTOR DEVICE WITH GLUE LAYER IN OPENING

On page 1, starting in 6, please replace the following with the following amended paragraph:

-- CROSS-REFERENCE TO RELATED APPLICATIONS ~~BACKGROUND OF THE INVENTION~~ --

On page 1, starting in 4, please add the following amended paragraphs: (Previously Amended)

--This application is a divisional of the application Serial No. 10/085,080 filed March 1, 2002, which is a ~~Divisional~~ divisional of ~~the~~ U.S. Patent Application ~~application Serial~~ No. 09/452,535, ~~now abandoned~~ filed January 27, 2000, ~~both of which claim priority to Japanese Patent Application No. 2001-095899, filed March 29, the entire contents all of which are incorporated herein by reference.~~ now abandoned.

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 11-16819, filed January 26, 1999, the entire contents of which are incorporated herein by reference.--

On page 1, starting in line 16, please replace the paragraph with the following amended paragraph:

--~~BRIEF~~ SUMMARY ~~OF THE INVENTION~~ --

On page 1, just above line 17, please add the following new paragraph:

-- A semiconductor device according to an aspect of the present invention comprises: an element isolation region in a semiconductor substrate and an active area in the semiconductor substrate, the element isolation region isolating the active area in the semiconductor substrate and the active area overlapping a top surface of the isolation region; an interlayer insulation film on the element isolation region and the active area; an opening to which the element isolation region, the active area and a boundary therebetween being exposed; a glue layer in the opening; and a conductor on the glue layer.--

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Cancelled)

2. (Previously Cancelled)

3. (Previously Cancelled)

4. (Previously Cancelled)

5. (Previously Cancelled)

6. (Previously Cancelled)

7. (Cancel)

8. (Cancel)

9. (Newly Added) A semiconductor device comprising:

an element isolation region in a semiconductor substrate and an active area in the semiconductor substrate, the element isolation region isolating the active area in the semiconductor substrate, and the active area overlapping a top surface of the isolation region;

an interlayer insulation film on the element isolation region and the active area and

having an opening to which the element isolation region, the active area and a boundary therebetween are exposed;

a glue layer in the opening; and

a conductor on the glue layer.

10. (Newly Added) The device according to claim 9, wherein the conductor is a metal layer.

11. (Newly Added) The device according to claim 10, wherein the metal layer contains tungsten.

12. (Newly Added) The device according to claim 9, wherein the glue layer contains an acid-resistant conductor.

13. (Newly Added) The device according to claim 9, wherein the glue layer contains titanium.

14. (Newly Added) The device according to claim 9, wherein the glue layer contains titanium nitride.

15. (Newly Added) The device according to claim 9, wherein the glue layer contains a layered film of titanium and titanium nitride.

16. (Newly Added) The device according to claim 9, further comprising a reaction layer of a metal layer on a surface of the active area.

17. (Newly Added) The device according to claim 16, wherein the reaction layer is a silicide layer.

18. (Newly Added) The device according to claim 17, wherein the silicide layer contains titanium and silicon.

19. (Newly Added) A semiconductor device comprising:

an element isolation region in a semiconductor substrate, the element isolation region isolating an active area in the semiconductor substrate;

a semiconductor layer on a top surface of the active area, the semiconductor layer overlapping the element isolation region;

an interlayer insulation film on the element isolation region and the semiconductor layer and having an opening to which the element isolation region, the semiconductor layer and a boundary therebetween are exposed;

a glue layer in the opening; and

a conductor on the glue layer.

20. (Newly Added) The device according to claim 19, wherein the conductor is a metal layer.

21. (Newly Added) The device according to claim 20, wherein the metal layer contains tungsten.

22. (Newly Added) The device according to claim 19, wherein the glue layer contains an acid-resistant conductor.

23. (Newly Added) The device according to claim 19, wherein the glue layer contains titanium.

24. (Newly Added) The device according to claim 19, wherein the glue layer contains titanium nitride.

25. (Newly Added) The device according to claim 19, wherein the glue layer contains a layered film of titanium and titanium nitride.

26. (Newly Added) The device according to claim 19, further comprising a reaction layer of a metal layer on a surface of the active area.

27. (Newly Added) The device according to claim 26, wherein the reaction layer is a silicide layer.

28. (Newly Added) The device according to claim 27, wherein the silicide layer contains titanium and silicon.

29. (Newly Added) A semiconductor device comprising:

an element isolation region in a semiconductor substrate, the element isolation region isolating an active area in the semiconductor substrate and having a hollow in the element isolation region to which a side surface of the active area faces;

a semiconductor layer in the hollow;

an interlayer insulation film on the element isolation region and the semiconductor layer and having an opening to which the element isolation region, the semiconductor layer and a boundary therebetween are exposed;

a glue layer in the opening; and

a conductor on the glue layer.

30. (Newly Added) The device according to claim 29, wherein the conductor is a metal layer.

31. (Newly Added) The device according to claim 30, wherein the metal layer contains tungsten.

32. (Newly Added) The device according to claim 29, wherein the glue layer contains an acid-resistant conductor.

33. (Newly Added) The device according to claim 29, wherein the glue layer contains titanium.

34. (Newly Added) The device according to claim 29, wherein the glue layer contains titanium nitride.

35. (Newly Added) The device according to claim 29, wherein the glue layer contains a layered film of titanium and titanium nitride.

36. (Newly Added) The device according to claim 29, further comprising a reaction layer of a metal layer on a surface of the active area.

37. (Newly Added) The device according to claim 36, wherein the reaction layer is a silicide layer.

38. (Newly Added) The device according to claim 37, wherein the silicide layer contains titanium and silicon.

REMARKS

Please enter this amendment before initial examination of this application.

The following brief explanation is provided to aid the Examiner's efficiency in examining the claims. There are three independent claims: 9, 19 and 29. Claim 9 describes the structure shown in FIG. 2, by using an expression such as "the active area overlapping a top surface of the isolation region". Claim 19 recites a semiconductor device. The device has the above-mentioned structure, and includes "a semiconductor layer on a top surface of the active area and overlapping the element isolation region". Claim 29 also recites a semiconductor device with the above-mentioned structure, and includes "a hollow in the element isolation region to which a side surface of the active area and a semiconductor layer in the hollow".

Claims 10 and 11 are related to metal, which generates "acid" during the manufacturing process. The metal requires a glue layer because it generates "acid" during the manufacturing process. Claims 12-15 recite the feature that the glue layer is acid-resistant.

Claims 16-18 are related to a metal reaction layer. Forming a metal reaction layer makes it easier for the active area to overlap the top surface of the isolation region.

Dependent claims 20-28 and dependent claims 30-38 recite limitations similar to those set forth in dependent claims 10-18.

An examination on the merits is solicited.

Respectfully submitted,

Pillsbury Winthrop, LLP

By: _____

Glenn J. Perry
Reg. No.: 28,458
Telephone: (703) 905-2161
Direct Fax: (703) 738-2277

Pillsbury Winthrop, LLP
1600 Tysons Boulevard
McLean, Virginia 22102

Switchboard: (703) 905-2000
Office fax: (703) 905-2500

Appendix A

Abstract

A semiconductor device includes: an element isolation region in a semiconductor substrate; an active area in the semiconductor substrate; an interlayer insulation film on the element isolation region and the active area; an opening to which the element isolation region, the active area and a boundary therebetween are exposed; a glue layer in the opening; and a conductor on the glue layer. The element isolation region isolates the active area in the semiconductor substrate, and the active area overlaps a top surface of the isolation region.